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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,630	03/31/2004	Atsuhiro Yamashita	65933-085	3848

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EXAMINER	
MA, CALVIN	
ART UNIT	PAPER NUMBER
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,630	YAMASHITA, ATSUHIRO	
	Examiner	Art Unit	
	Calvin Ma	2609	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,13,15,17 and 19* is/are rejected.

7)☒ Claim(s) *10,12,14,16,18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/31/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The reference H10(1998)-312173 cited on the specification on page 3, line 1 should be provided so that it can be considered.

3. The reference listed on the information disclosure statement filed on 08/31/2005 have been considered. (see attached PTO-1449)

Claim Objections

4. Claims 2-4 and 7-8 are objected to because of the following informalities:

Claim 2 recites "a transistor" in line 2. It would be better that the limitation "a transistor" in claim 2 is recited as "an adjustment transistor", and at subsequent claims 3 and 4 the limitation "the transistor" is changed to "adjustment transistor" because it is not clear whether "the transistor" recited in claim 3 is referred either to "driving transistor" or "adjustment transistor". Thus, this change makes claims read better. Appropriate correction is required.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims1, 2, 4, 5, 6, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hanari et al. (U.S.P.G. Pub 2003/0063078)

Consider claim 1, Hanari discloses a digital-driven display element (Fig 1-2) comprising:

- a light emitting element (16) which emits light when an electric current is supplied thereto [0015] ;
- a driving transistor (17) which controls the supply of the electric current to the light emitting element (16) and is operated in a linear region ([0008] the driving thin-film transistor (there of TFT) is said to be operated in the saturation region, which refers to the linear region that transistor has to operate under to reach saturation region); and
- an electric current adjustment element (14) which is connected to the light emitting element (16) and the driving transistor (17) in series (in Fig. 1 the current adjustment element-dimmer clearly connect the power supply 12, with the organic EL panel 10, which is further explained in Fig. 2, where the power line VDD from the dimmer is

connected to 17 the driving transistor), to adjust the electric current flowing through the light emitting element (16) (see paragraph [0063], it is stated that dimmer switch equally switches driving currents flowing in organic EL elements this is essentially adjusting current for the driving transistor in Fig. 1, the dimmer 14 is connected to a controller 13, which refers to the multi-state adjustability of the dimmer itself).

Consider claim 2, Hanari clearly teaches the display element according to claim 1, where in a switching transistor (14) as the electric current adjustment element (see paragraph [0054] it is clearly stated that thin-film transistors are formed as the dimmer switch).

Consider claim 4, Hanari clearly teaches the display element according to claim 2, wherein

- a control signal (SC) for variably controlling the electric current flowing through the light emitting element (16) is inputted to a gate electrode of the transistor(14) (as mentioned in claim 3 the TFT functioning as the adjustment unit in dimmer connects to the controller 13 which is inputting to the gate of the TFT, even if the control signals goes to the source or drain of the TFT the gate still must to be controlled indirectly by the controller 13 in order for the TFT to function as the dimmer for the EL display; further more, Fig. 8 clearly shows the control signal SC is inputted to the gate of the transistor 22).

Consider claim 5, 6, and 8 Hanari clearly teaches the display elements arranged in a matrix (see Fig. 9, [0048]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3, 7 are rejected under 35 U.S.C. 103(e) as being unpatentable over U.S.P.G. Pub 2003/0063078 to Hanari et al. in view of Nishitoba et al. (US Patent Number 6,774,877)

Consider claim 3, Hanari teaches the display element in claim 2, Hanari does not teach wherein a signal same as that inputted to a gate electrode of the driving transistor is inputted to a gate electrode of the transistor. Nishitoba (Fig 3) teaches wherein a signal same as that inputted to a gate electrode of the driving transistor (8) is inputted to a gate electrode of the transistor(9) (see Column 6, Line 40-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the current mirror structure of Nishitoba in addition to Hanari's since it, "allows a current driver circuit to be obtained that can drive an element accurately based on a signal current therefore allows an improvement in the picture quality of a display image". (Column 4, Lines 53-57 of Nishitoba)

Consider claim 7, Hanari clearly teaches the implementation of claim 3 arranged in a matrix (see Fig. 7).

10. Claims 9, 11, 13, 15 are rejected under 35 U.S.C. 103(e) as being unpatentable over U.S.P.G. Pub 2003/0063078 to Hanari et al. in view of Hunter et al. (U.S.P.G. Pub 2003/0098828)

Consider claim 9, Hanari clearly teaches a digital-driven display device comprising:

- a plurality of pixel circuits (PX), each of the plurality of pixel circuits comprising
- a light emitting element (16) which emits light when an electric current is supplied thereto (see paragraph [0050]) ;
- a driving transistor (17) which controls the supply of the electric current to the light emitting element (16) and is operated in a linear region ([0008] the driving TFT is said to

be operated in the saturation region, which refers to the linear region that transistor has to operate under to reach saturation region); and

- a power source line (VDD) through which the electric current is supplied to the light emitting element (16) of each pixel circuit,
- an electric current adjustment element (14) which is connected to the light emitting element (16) and the driving transistor (17) in series (in Fig. 1 the current adjustment element-dimmer clearly connect the power supply 12, with the organic EL panel 10, which is further explained in Fig. 2, where the power line VDD from the dimmer is connected to 17 the driving transistor), to adjust the electric current flowing through the light emitting element (16) see paragraph [0063] it is stated that dimmer switch equally switches driving currents flowing in organic EL elements, this is essentially adjusting current for the driving transistor considering in figure 1 the dimmer 14 is connected to a controller 13 which refers to the multi-state adjustability of the dimmer itself).

Hanari does not teach

- the power source line branching from a first power source on a side of high electric potential to each pixel circuit at a first node, and converging from each pixel circuit at a second node, and then being connected to a second power source on a side of low electric potential, and
- an electric current adjustment circuit which adjusts the electric current flowing through the light emitting element being disposed between the first node and the first power source.

Hunter teaches

- the power source line branching from a first power source (30 and 32) on a side of high electric potential to each pixel circuit at a first node (a node located at the capacitor 24), and converging from each pixel circuit at a second node (a node located at the transistor 16) and then being connected to a second power source (42) on a side of low electric potential see Fig. 3 and [0040-0041], and

- an electric current adjustment circuit (32a) which adjusts the electric current flowing through the light emitting element (2) being disposed between the first node and the first power source (30 and 32, as seen in Fig. 3 the switch 32a regulate the power source and therefore adjust the circuit).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the dual power source structure of Hunter in addition to Hanari's because dual power source of Hunter "enables the display to have a low power standby mode". (page 1, 0009)

Consider claim 11, this claim differs from claim 9 only in that the limitation

- "an electric current adjustment circuit which adjusts the electric current flowing through the light emitting element being disposed between the second node and the second power source" is recited instead of "between the first node and the second power source" as recited in claim 9.

Hunter teaches

- an electric current adjustment circuit (40) which adjusts the electric current flowing through the light emitting element being disposed between the second node and the second power source (42, as seen in Fig. 3 the switch next to the second power source 42 regulate the power source and therefore adjust the circuit).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the dual power source structure of Hunter in addition to Hanari's for the same reasons as discussed in claim 9 above.

Consider claim 13 and 15 Hanari teaches switching transistor (14) as the electric current adjustment element (see paragraph [0054], it is clearly stated that thin-film transistors are formed as the dimmer switch).

11. Claim 17, 19, are rejected under 35 U.S.C. 103(e) as being unpatentable over U.S.P.G. Pub 2003/0063078 to Hanari et al. in view of Moya et al. (U.S. Patent Number 6,469,405)

Consider claim 17 and 19 note the discussion of Hanari above, Hanari does not teach wherein the electric current adjustment circuit is a resistor. Moya does teach wherein the electric current adjustment circuit is a resistor (Figure 14, Column 19, Lines 55-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the resistor based adjustment structure with the switching element of Hanari because it reduces "the effect of switching noises". (Column 4, Lines 49-50 of Moya)

Allowable Subject Matter

12. Claims 10, 12, 14, 16, 18, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Prior art Miyazawa (U.S. P.G. Pub 2004/0222986) is cited to teach a device similar to what the applicant's disclosed device. However, it does not precede the original Japanese priority date of the application.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Calvin Ma whose telephone number is (571) 270-1713. The examiner can normally be reached on Monday - Friday 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma
January 24, 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER